AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original): A method of forming a thin film transistor, comprising:

forming a buffer layer on a transparent substrate;

forming an amorphous silicon layer on the buffer layer;

crystallizing the amorphous silicon layer into a polysilicon layer using a sequential lateral solidification (SLS) method;

patterning the polysilicon layer to form a polysilicon active layer;

performing a rapid thermal annealing (RTA) process to the polysilicon active layer under a H_2 atmosphere;

performing a rapid thermal oxidation (RTO) process to form a silicon-oxidized layer on the polysilicon active layer after the RTA process; and

forming a metal layer over the transparent substrate to cover the silicon-oxidized layer.

2. (Currently Amended): A method of forming a thin film transistor, comprising:

forming a buffer layer on a transparent substrate;

forming an amorphous silicon layer on the buffer layer;

crystallizing the amorphous silicon layer into a polysilicon layer using a sequential lateral solidification (SLS) method;

patterning the polysilicon layer to form a polysilicon active layer;

performing a rapid thermal annealing (RTA) process to the polysilicon active layer under a H_2 atmosphere;

performing a rapid thermal oxidation (RTO) process to form a silicon-oxidized layer on the polysilicon active layer after the RTA process;

forming a metal layer over the transparent substrate to cover the silicon-oxidized layer;

patterning the metal layer to form a gate electrode over the polysilicon active layer;

doping the [[ploysilicon]]polysilicon active layer with impurities using the gate electrode as a doping mask to form ohmic contact regions;

forming an interlayer insulator over the transparent substrate to cover the gate electrode;

patterning the interlayer insulator to form first and second contact holes exposing the ohmic contact regions;

forming source and drain electrodes on the interlayer insulator, the source and drain electrodes contacting the ohmic contact regions, respectively, through the first and second contact holes;

forming a passivation layer on the interlayer [[insulation]]insulator to cover the source and drain electrodes, wherein the passivation layer has a drain contact hole that exposes a portion of the drain electrode; and

forming a pixel electrode on the passivation layer, the pixel electrode contacting the drain electrode through the drain contact hole.

3. (Original): The method according to claim 2 , wherein the patterning the metal layer includes patterning the silicon-oxidized layer into the same shape as the gate electrode.

4. (Original): The method according to claim 2, wherein the interlayer insulator is formed of one of silicon oxide and silicon nitride.

5. (Currently Amended): The method according to claim 2, wherein the RTA and RTO processes are conducted at a temperature in the range of about 500 to 1000 degrees Celsius [[(ÿ)]].

6. (Previously Presented): The method according to claim 2, wherein the RTA and RTO processes are conducted for less than 60 minutes.

7. (Previously Presented): The method according to claim 2, wherein the RTO process is conducted under an oxygen-based atmosphere.

8. (Original): The method according to claim 7, wherein the oxygen-based atmosphere includes at least one of O_2, N_2O, and NO.

9. (Previously Presented): The method according to claim 2, further comprising dehydrogenating the amorphous silicon layer before crystallizing the amorphous silicon layer.

10. (Previously Presented): The method according to claim 2, wherein the metal layer is selected from the group consisting of aluminum (Al), aluminum alloy (Al-alloy), and molybdenum (Mo).

11. (Previously Presented): The method according to claim 2, wherein the crystallizing the amorphous silicon layer generates a plurality of protuberances of the polysilicon layer.

12. (Currently Amended): The method according to claim [[2]]11, wherein the RTA process blunts and flattens the protuberances of the polysilicon layer.